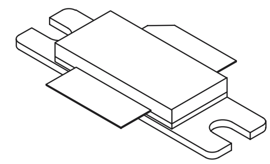
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF18085A
MRF18085AR3
MRF18085ALSR3

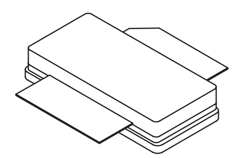
Designed for GSM and GSM EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications. Specified for GSM–GSM EDGE 1805 – 1880 MHz.

- GSM and GSM EDGE Performance, Full Frequency Band (1805–1880 MHz)
  Power Gain – 15 dB (Typ) @ 85 Watts CW
  Efficiency – 52% (Typ) @ 85 Watts CW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 26 Vdc, @ P1dB Output Power, @ f = 1805 MHz
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.
- Available with Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ″ Nominal.

GSM/GSM EDGE
1.8 – 1.88 GHz, 85 W, 26 V
LATERAL N–CHANNEL
RF POWER MOSFETs



CASE 465–06, STYLE 1
NI–780
MRF18085A, MRF18085AR3



CASE 465A–06, STYLE 1
NI–780S
MRF18085ALSR3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	273 1.56	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.64	°C/W

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Typical)
Machine Model	M3 (Typical)

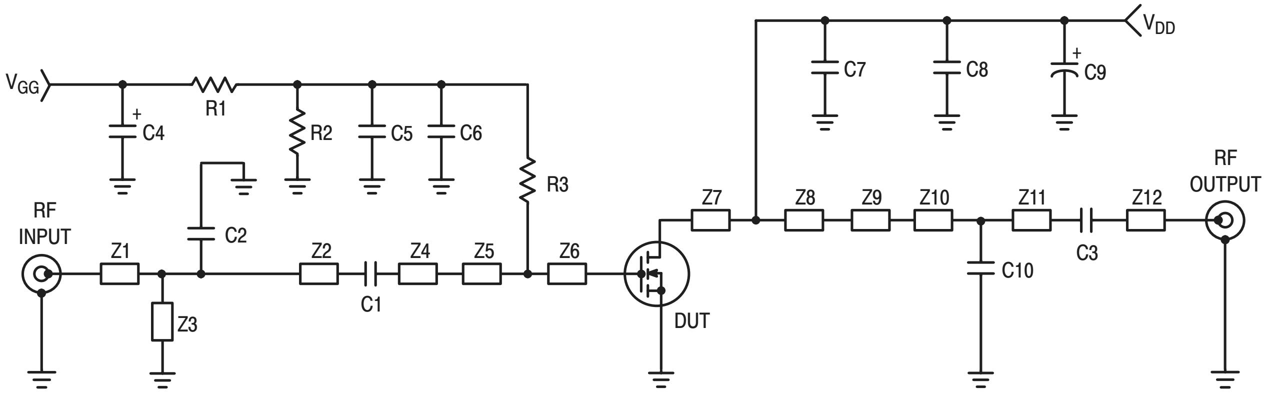
NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 0

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 600 mAdc)	$V_{GS(Q)}$	2.5	3.9	4.5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2 Adc)	$V_{DS(on)}$	—	0.15	—	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	6.0	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance (1) (V_{DS} = 26 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	3.6	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Common–Source Amplifier Power Gain @ 85 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1805 – 1880 MHz)	G_{ps}	13.5	15	—	dB
Drain Efficiency @ 85 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1805 – 1880 MHz)	η	48	52	—	%
Input Return Loss @ 85 W (2) (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1805 – 1880 MHz)	IRL	—	–12	–9	dB
P_{out}, 1 dB Compression Point (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1805 – 1880 MHz)	P1dB	83	90	—	Watts
Output Mismatch Stress @ P1dB (V_{DD} = 26 Vdc, I_{DQ} = 800 mA, f = 1805 MHz, VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.
(2) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch–to–batch consistency.



C1, C3, C6, C7	10 pF Chip Capacitors, B Case, ATC	Z4	0.610″ x 00.118″ Microstrip
C2	1.8 pF Chip Capacitor, B Case, ATC	Z5	0.331″ x 1.153″ Microstrip
C4	10 μF, 35 V Tantalum Capacitor, AVX	Z6	0.063″ x 1.153″ Microstrip
C5, C8	1 nF Chip Capacitors, B Case, ATC	Z7	0.122″ x 0.925″ Microstrip
C9	220 μF, 63 V Electrolytic Capacitor, Radial, Philips	Z8	0.547″ x 0.925″ Microstrip
C10	0.3 pF Chip Capacitor, B Case, ATC	Z9	0.394″ x 0.177″ Microstrip
R1, R2	10 kΩ, 1/4 W Chip Resistors (1206)	Z10	0.180″ x 0.087″ Microstrip
R3	1.0 kΩ, 1/4 W Chip Resistor (1206)	Z11	0.686″ x 0.087″ Microstrip
Z1	0.671″ x 0.087″ Microstrip	Z12	0.294″ x 0.087″ Microstrip
Z2	0.568″ x 0.087″ Microstrip	PCB	Taconic TLX8, 0.8 mm Thickness
Z3	0.500″ x 0.098″ Microstrip Shorted Stub	Connectors	“N” Type, Macom 3052–1648–10

Figure 1. 1.80 – 1.88 GHz Test Fixture Schematic

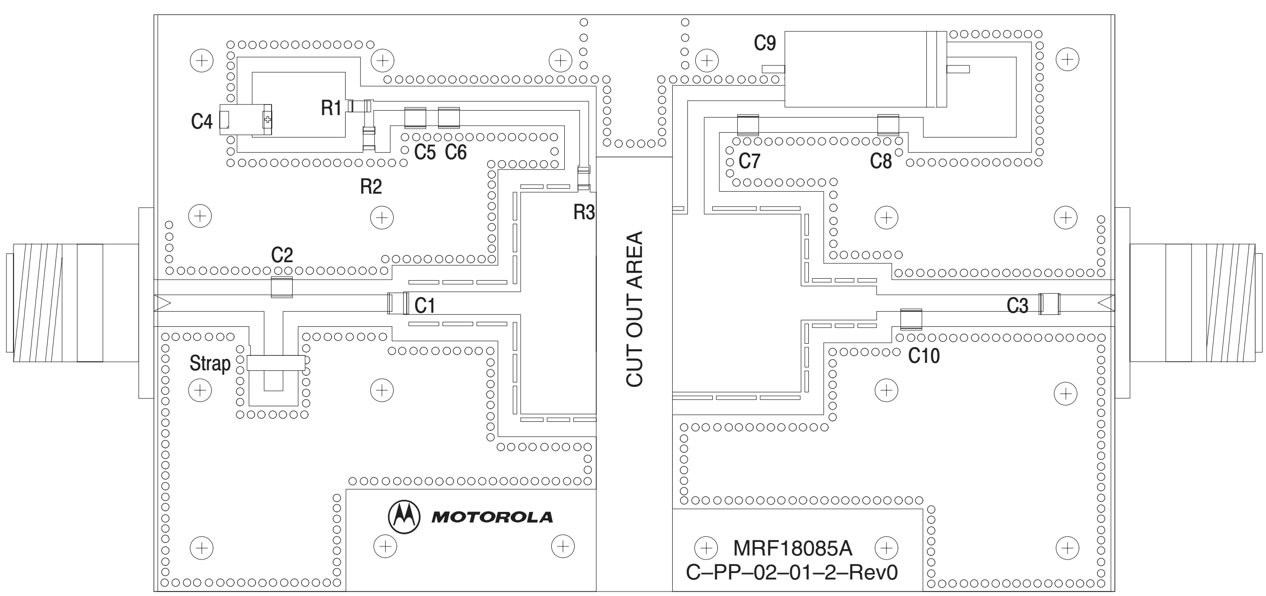


Figure 2. 1.80 – 1.88 GHz Test Fixture Component Layout

TYPICAL CHARACTERISTICS

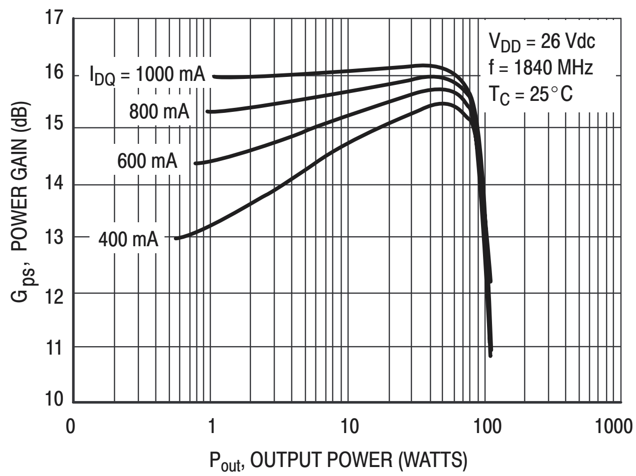


Figure 3. Power Gain versus Output Power

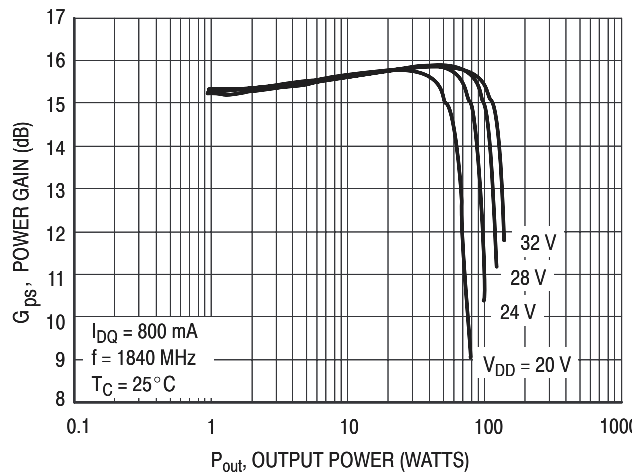


Figure 4. Power Gain versus Output Power

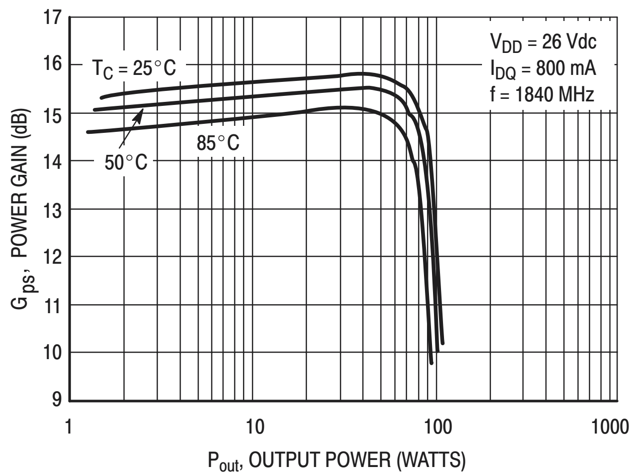


Figure 5. Power Gain versus Output Power

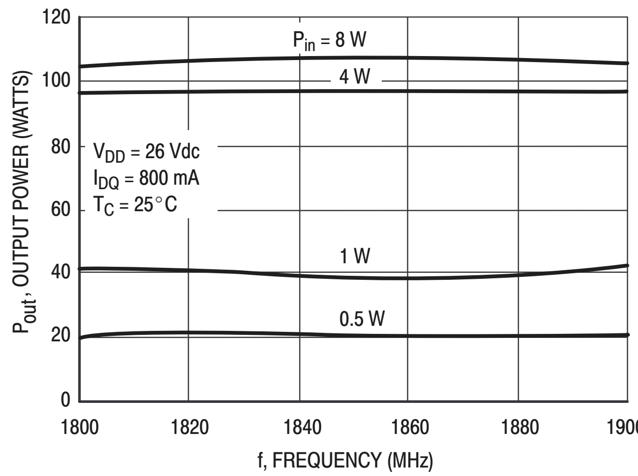


Figure 6. Output Power versus Frequency

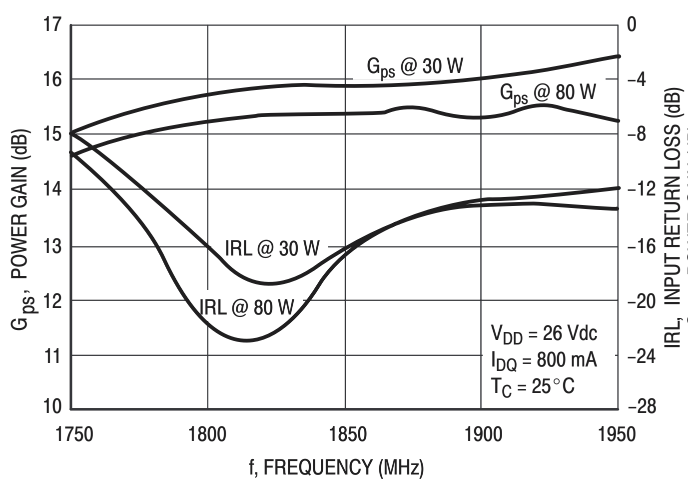


Figure 7. Power Gain versus Frequency

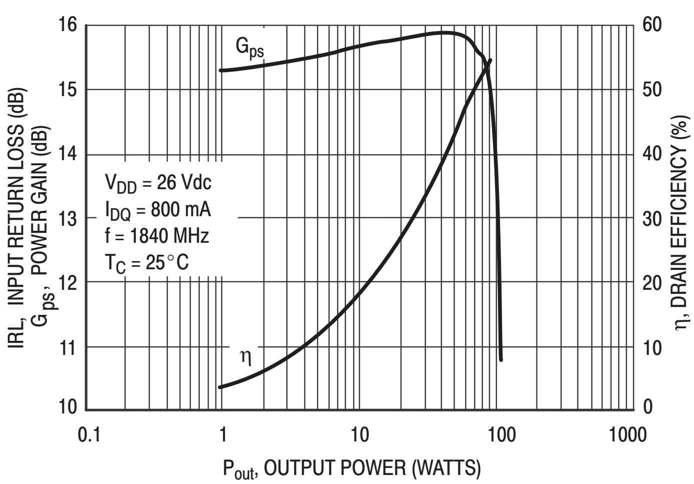
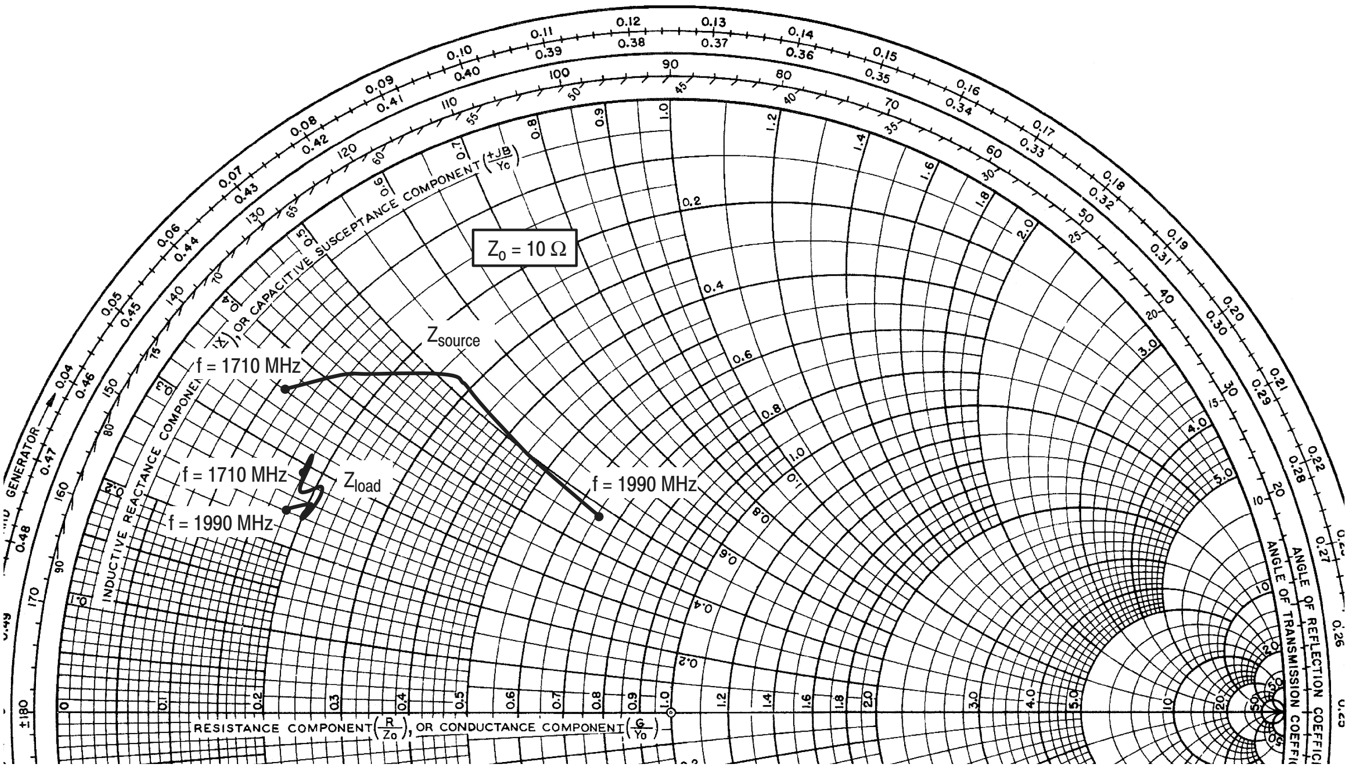


Figure 8. Power Gain and Efficiency versus Output Power



V_{DD} = 26 V, I_{DQ} = 800 mA, P_{out} = 85 W CW

f MHz	Z_{source} Ω	Z_{load} Ω
1710	1.13 + j3.62	1.79 + j2.88
1785	1.61 + j4.23	1.82 + j3.15
1805	1.69 + j4.34	1.90 + j2.66
1880	2.83 + j5.25	2.09 + j2.77
1930	3.00 + j5.18	2.01 + j2.44
1960	4.39 + j4.97	2.01 + j2.57
1990	6.59 + j4.74	1.79 + j2.37

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

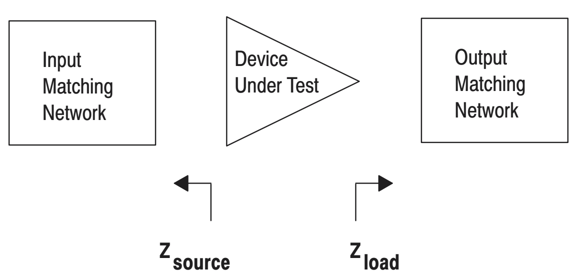
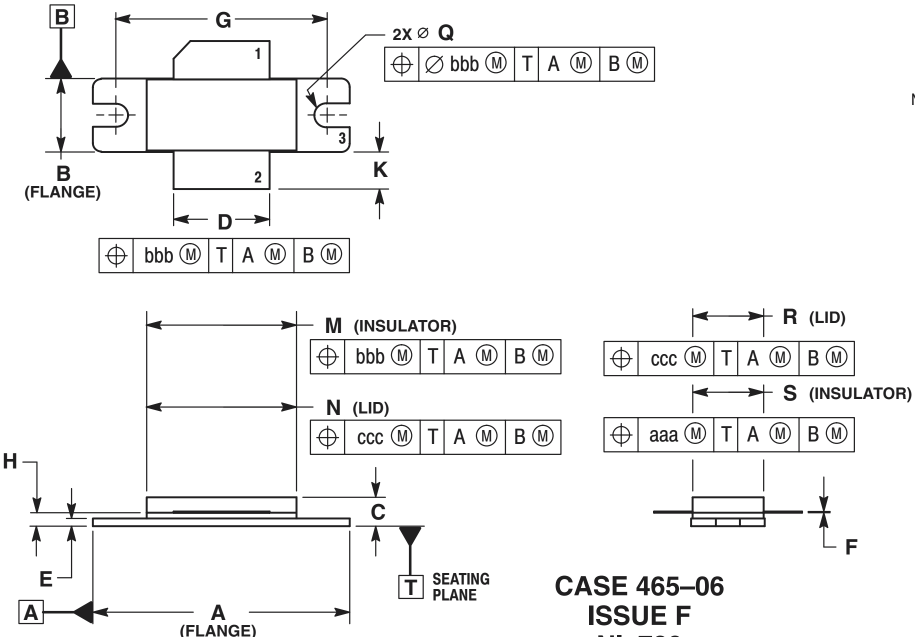


Figure 9. Series Equivalent Input and Output Impedance

NOTES

PACKAGE DIMENSIONS

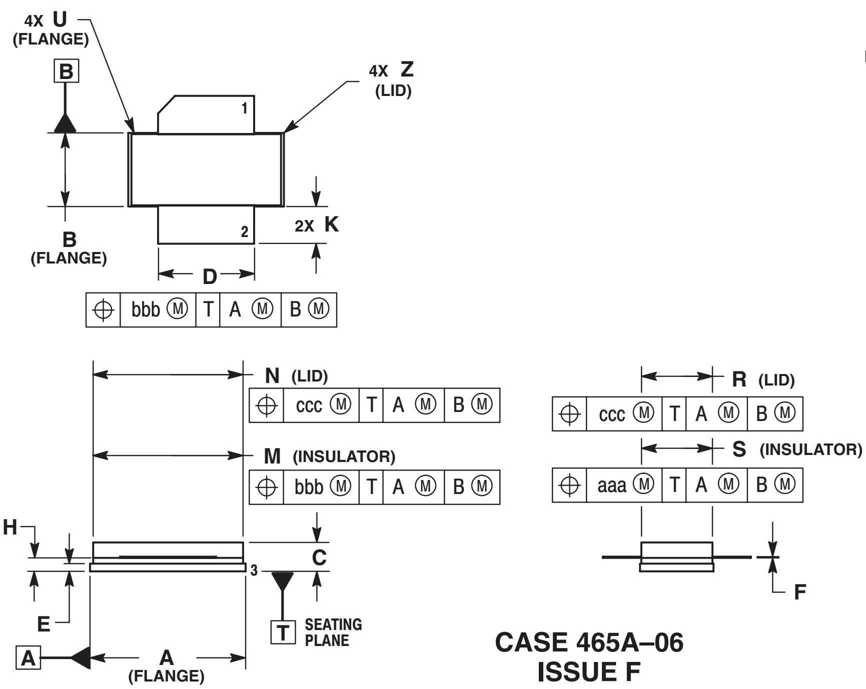


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M–1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	∅.118	∅.138	∅3.00	∅3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465–06
ISSUE F
NI–780
MRF18085A, MRF18085AR3



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3. DELETED
4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
5. SOURCE

CASE 465A–06
ISSUE F
NI–780S
MRF18085ALSR3

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